

**What is claimed is:**

1           1.    A control thin film transistor for controlling  
2    an organic light-emitting diode (OLED), comprising:  
3           a substrate;  
4           a semiconductor layer disposed on the substrate as a  
5           channel region;  
6           a first and second doped region sequentially  
7           disposed on a first side of the semiconductor  
8           layer, wherein the doped concentration of the  
9           first doped region is lower than that of the  
10          second doped region, and the first doped region  
11          serves as a single-side lightly doped drain  
12          region and the second doped region serves as a  
13          drain region;  
14          a third doped region disposed on a second side of  
15          the semiconductor layer, which is opposite to  
16          the first side, serving as a source region;  
17          an insulating layer disposed on the surface of the  
18          semiconductor layer, and the first, second, and  
19          third regions;  
20          a source and drain electrode penetrating the  
21          insulating layer contacting the source and  
22          drain regions respectively, wherein the drain  
23          electrode receives a drain voltage and the  
24          source electrode is electrically connected to  
25          an OLED unit; and  
26          a conductive layer serving as a gate layer disposed  
27          in the insulating layer, at approximately the  
28          top right portion of the semiconductor layer.

1           2.    The control thin film transistor as claimed in  
2           claim 1, wherein the semiconductor layer is composed of  
3           polysilicon.

1           3.    The control thin film transistor as claimed in  
2           claim 1, wherein the first, second and third doped  
3           regions are n-type doped.

1           4.    The control thin film transistor as claimed in  
2           claim 1, wherein the first, second and third doped  
3           regions are p-type doped.

1           5.    The control thin film transistor as claimed in  
2           claim 1, wherein the first, second and third doped  
3           regions are mainly composed of silicon.

1           6.    A control thin film transistor for controlling  
2           an organic light-emitting diode (OLED), comprising:

3           a substrate;

4           a semiconductor layer disposed on the substrate as a  
5           channel region;

6           a first and second doped region sequentially  
7           disposed on a first side of the semiconductor  
8           layer, wherein the doped concentration of the  
9           first doped region is lower than that of the  
10          second doped region, and the second doped  
11          region serves as a drain region;

12          a third and fourth doped region sequentially  
13          disposed on a second side of the semiconductor  
14          layer, which is opposite to the first side;  
15          wherein the doped concentration of the third

16                   doped region is lower than that of the fourth  
17                   doped region that serves as a source region and  
18                   the length of the third doped region is less  
19                   than that of the first doped region;  
20           an insulating layer disposed on the surface of the  
21           semiconductor layer, and the first, second,  
22           third and fourth regions;  
23           a source and drain electrode penetrating the  
24           insulating layer contacting the source and  
25           drain regions respectively, wherein the drain  
26           electrode receives a drain voltage and the  
27           source electrode is electrically connected to  
28           an OLED unit; and  
29           a conductive layer serving as a gate layer disposed  
30           in the insulating layer, at approximately the  
31           top right portion of the semiconductor layer.

1           7.   The control thin film transistor as claimed in  
2           claim 6, wherein the semiconductor layer is composed of  
3           polysilicon.

1           8.   The control thin film transistor as claimed in  
2           claim 6, wherein the first, second, third and fourth  
3           doped regions are n-type doped.

1           9.   The control thin film transistor as claimed in  
2           claim 6, wherein the first, second, third and fourth  
3           doped regions are p-type doped.

1           10.  The control thin film transistor as claimed in  
2           claim 6, wherein the first, second, third and fourth  
3           doped regions are mainly composed of silicon.

1           11. An electroluminescent display device, which  
2 sequentially scans a plurality of pixels composing a  
3 display screen and provides current to the scanned pixels  
4 according to pixel signals received while scanning,  
5 thereby activating electroluminescent units in the pixels  
6 to display figures on the display screen according to the  
7 pixel signals, the device is characterized by having a  
8 plurality of control TFTs as claimed in claim 1 in the  
9 pixels to control the current provided to the scanned  
10 pixels.

1           12. An electroluminescent display device, which  
2 sequentially scans a plurality of pixels composing a  
3 display screen and provides current to the scanned pixels  
4 according to pixel signals received while scanning,  
5 thereby activating electroluminescent units in the pixels  
6 to display figures on the display screen according to the  
7 pixel signals, the device is characterized by having  
8 plurality of control TFTs as claimed in claim 5 in the  
9 pixels to control the current provided to the scanned  
10 pixels.

1           13. A method of fabricating a control thin film  
2 transistor for controlling a current of an OLED unit,  
3 comprising the steps of:

4           providing a substrate;

5           forming and defining a semiconductor layer on the  
6           substrate;

7           forming a first photoresist layer covering a portion  
8           of the semiconductor layer, exposing

9                   predetermined portions on the semiconductor  
10                  layer for a source and drain regions;  
11           performing a first ion implantation of the  
12                  semiconductor layer using the first photoresist  
13                  layer as a mask to form the source and drain  
14                  regions thereon;  
15           removal of the first photoresist layer;  
16           forming a first insulating layer covering the  
17                  surface of the substrate and the semiconductor  
18                  layer;  
19           forming a second photoresist layer on the first  
20                  insulating layer, which covers the un-implanted  
21                  area of the semiconductor layer but exposes  
22                  only a portion of the un-implanted area of the  
23                  semiconductor layer adjacent to the drain  
24                  region;  
25           performing a second ion implantation of the  
26                  semiconductor layer using the second  
27                  photoresist layer as a mask to form a lightly  
28                  doped region with a doped concentration lower  
29                  than that of the adjacent drain region;  
30           removal of the second photoresist layer;  
31           forming a gate layer on the first insulating layer  
32                  and at approximately the right top of the un-  
33                  doped semiconductor layer;  
34           forming a second insulating layer covering the  
35                  surface of the first insulating layer and the  
36                  gate layer; and  
37           forming a source and drain electrodes penetrating  
38                  the first and second insulating layer in

39                   contact with the source and drain regions  
40                   respectively, wherein the drain electrode  
41                   receives a drain voltage and the source  
42                   electrode is electrically connected to an OLED  
43                   unit.

1           14. The method as claimed in claim 13, wherein  
2           forming the semiconductor layer further comprises the  
3           steps of:

4               forming an amorphous silicon layer on the substrate;  
5               and  
6               performing a laser treatment of the amorphous  
7               silicon layer to crystallize as a polysilicon  
8               layer as the semiconductor layer.

1           15. The method as claimed in claim 14, wherein  
2           dopants of the first and second ion implantation are n-  
3           type dopants.

1           16. The method as claimed in claim 14, wherein  
2           dopants of the first and second ion implantation are p-  
3           type dopants.

1           17. The method as claimed in claim 14, wherein the  
2           first and second insulating layers are silicon oxide.

1           18. A method of fabricating a control thin film  
2           transistor for controlling a current of an OLED unit,  
3           comprising the steps of:

4               providing a substrate;  
5               forming and defining a semiconductor layer on the  
6               substrate;

7           forming a first photoresist layer covering a portion  
8           of the semiconductor layer, exposing  
9           predetermined portions on the semiconductor  
10          layer for a source and drain region;  
11          performing a first ion implantation of the  
12          semiconductor layer using the first photoresist  
13          layer as a mask to form the source and drain  
14          regions thereon;  
15          removal of the first photoresist layer;  
16          forming a first insulating layer covering the  
17          surface of the substrate and the semiconductor  
18          layer;  
19          forming a second photoresist layer on the first  
20          insulating layer, which covers the un-implanted  
21          area of the semiconductor layer but exposes two  
22          portions of the un-implanted area of the  
23          semiconductor layer adjacent to the drain and  
24          source regions respectively, wherein the  
25          portion adjacent to the drain region is greater  
26          than the portion adjacent to the source region;  
27          performing a second ion implantation of the  
28          semiconductor layer using the second  
29          photoresist layer as a mask to form lightly  
30          doped drain and source regions with a dopant  
31          concentration lower than that of the adjacent  
32          drain and source regions respectively, wherein  
33          the lightly doped drain region is larger than  
34          the lightly doped source region;  
35          removal of the second photoresist layer;

36           forming a gate layer on the first insulating layer  
37                   and at approximately the right top of the un-  
38                   doped semiconductor layer;  
39           forming a second insulating layer covering the  
40                   surface of the first insulating layer and the  
41                   gate layer; and  
42           forming a source and drain electrodes penetrating  
43                   the first and second insulating layer in  
44                   contact with the source and drain regions  
45                   respectively, wherein the drain electrode  
46                   receives a drain voltage and the source  
47                   electrode is electrically connected to an OLED  
48                   unit.

1           19. The method as claimed in claim 18, wherein  
2           forming the semiconductor layer further comprises the  
3           steps of:

4                   forming an amorphous silicon layer on the substrate;  
5                   and  
6           performing a laser treatment of the amorphous  
7                   silicon layer to crystallize as a polysilicon  
8                   layer as the semiconductor layer.

1           20. The method as claimed in claim 19, wherein  
2           dopants of the first and second ion implantation are n-  
3           type dopants.

1           21. The method as claimed in claim 19, wherein  
2           dopants of the first and second ion implantation are p-  
3           type dopants.



1           22. The method as claimed in claim 19, wherein the  
2 first and second insulating layers are silicon oxide.